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LEE et al.(10) **Pub. No.: US 2019/0140038 A1**(43) **Pub. Date: May 9, 2019**(54) **ORGANIC LIGHT EMITTING DIODE
DISPLAY**(71) Applicant: **LG Display Co., Ltd.**, Seoul (KR)(72) Inventors: **Joonsuk LEE**, Paju-si (KR); **Sejune
KIM**, Paju-si (KR)(73) Assignee: **LG Display Co., Ltd.**, Seoul (KR)(21) Appl. No.: **16/181,579**(22) Filed: **Nov. 6, 2018**(30) **Foreign Application Priority Data**

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(57)

ABSTRACT

An organic light emitting diode display is disclosed. The organic light emitting diode display includes a first substrate on which a power electrode supplied with a power voltage and an organic light emitting diode are disposed, a second substrate on which a power line is disposed, the second substrate facing the first substrate, a conductive filler layer interposed between the first substrate and the second substrate, the conductive filler layer including a conductive medium electrically connecting a cathode of the organic light emitting diode to the power line, and a conductive sealant disposed at an edge of the first substrate and an edge of the second substrate, the conductive filler layer being accommodated inside the conductive sealant. The conductive sealant electrically connects the power electrode to the power line.

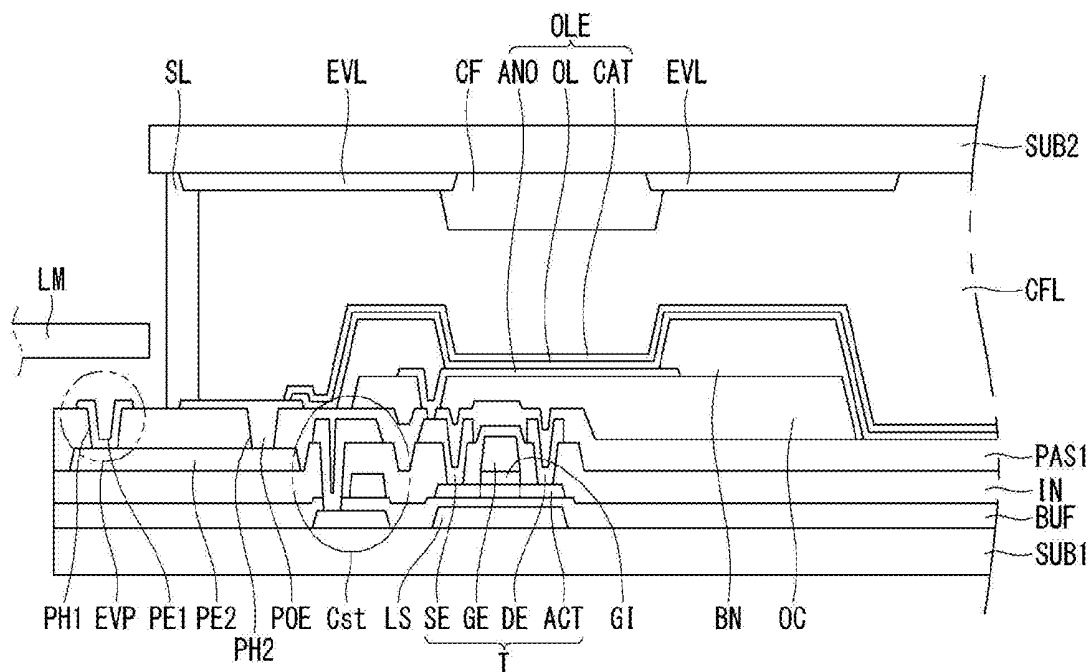


FIG. 1

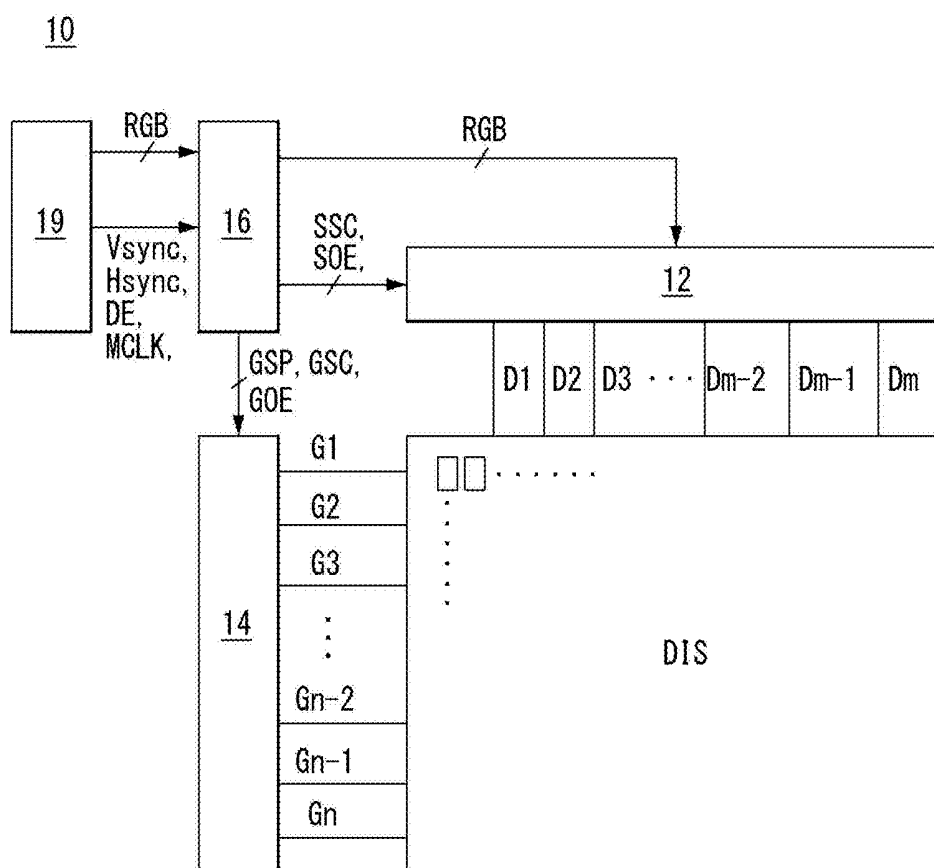


FIG. 2

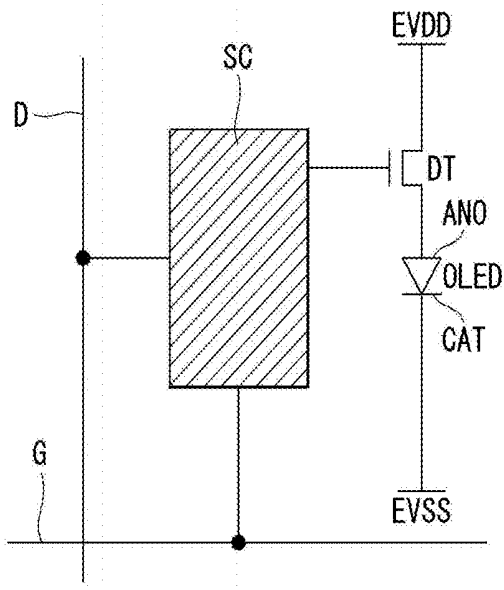


FIG. 3

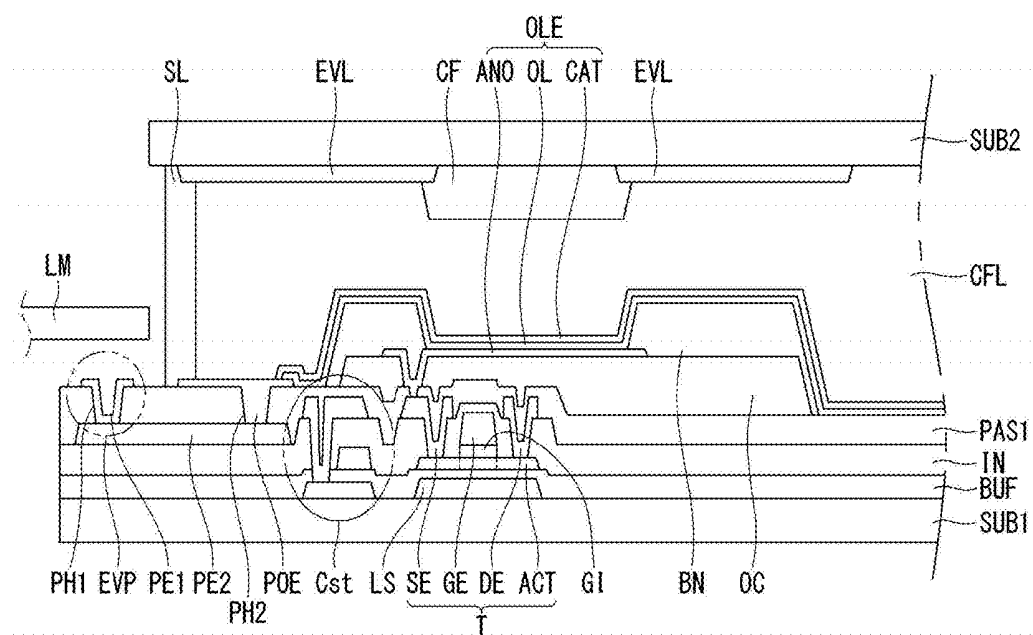


FIG. 4

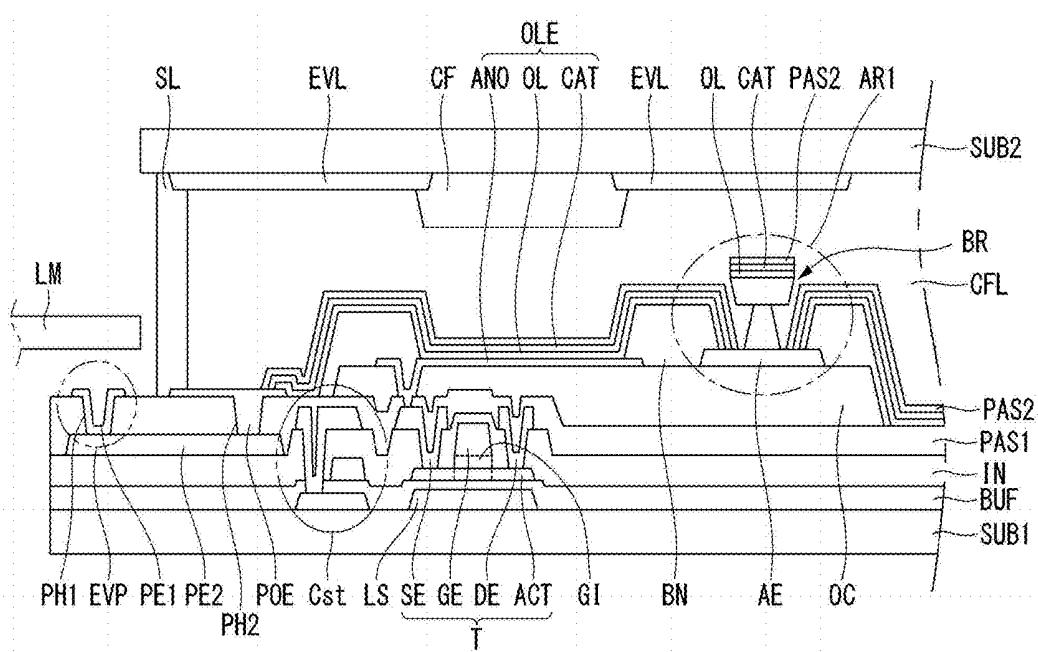


FIG. 5

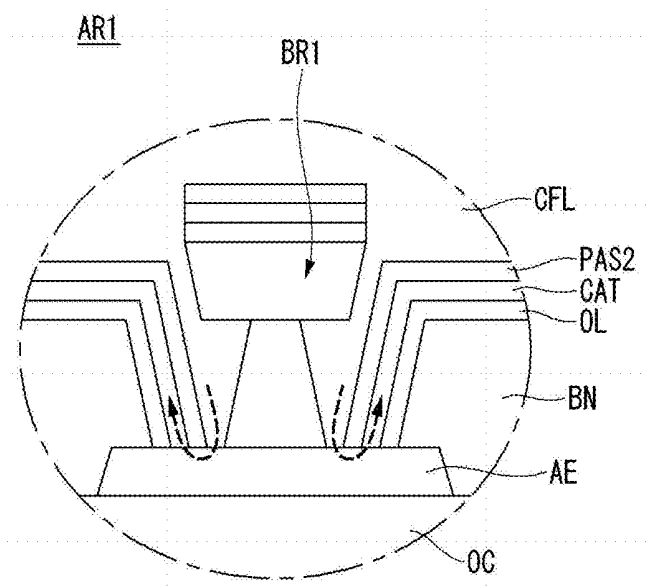


FIG. 6

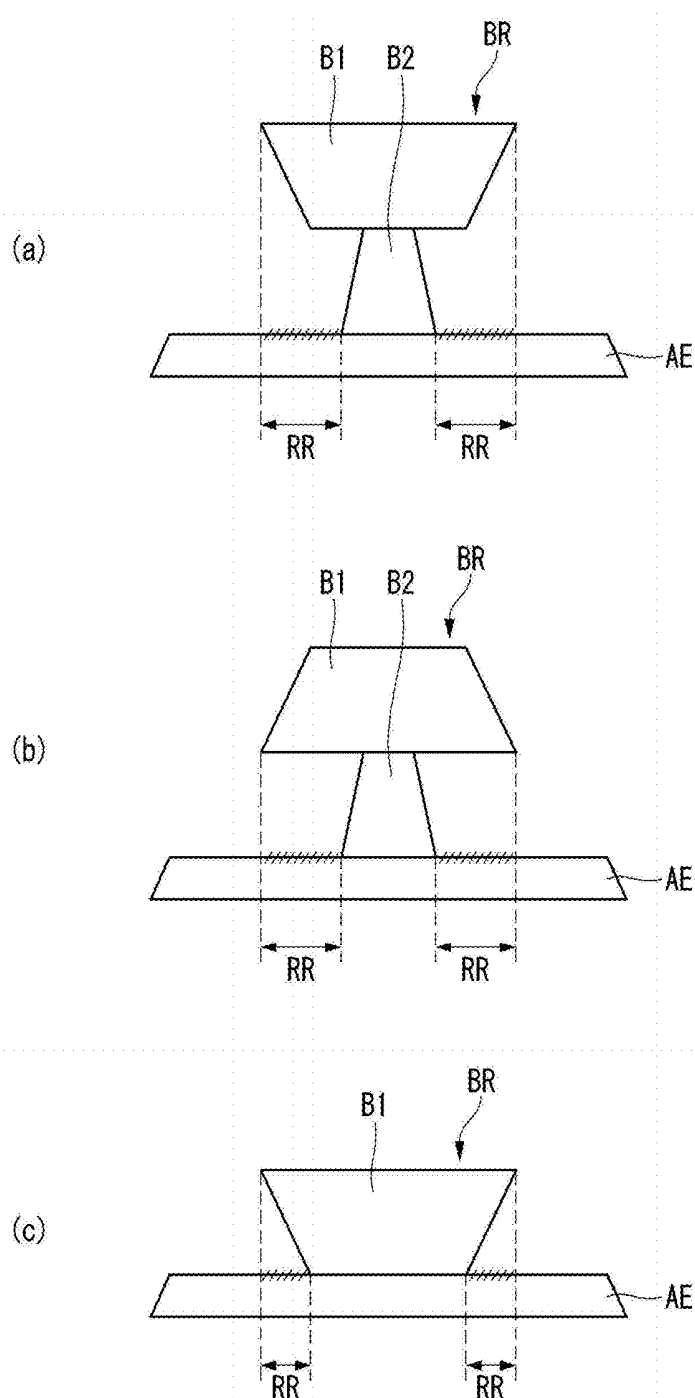


FIG. 7

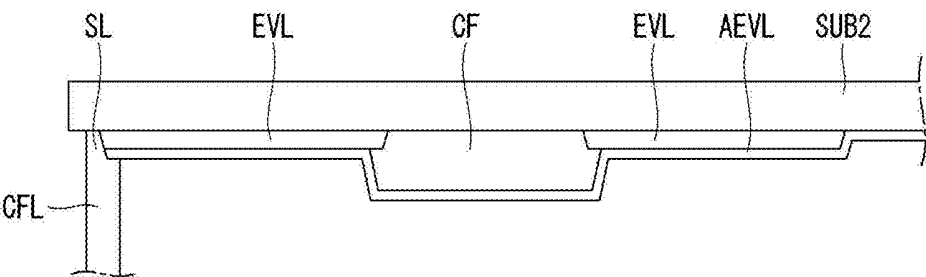


FIG. 8

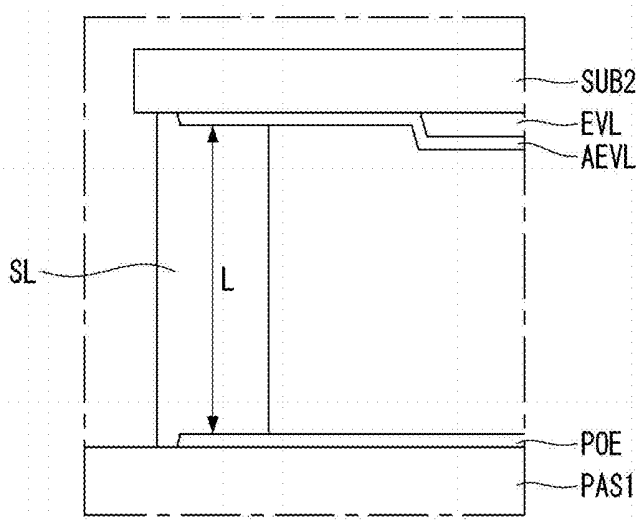


FIG. 9

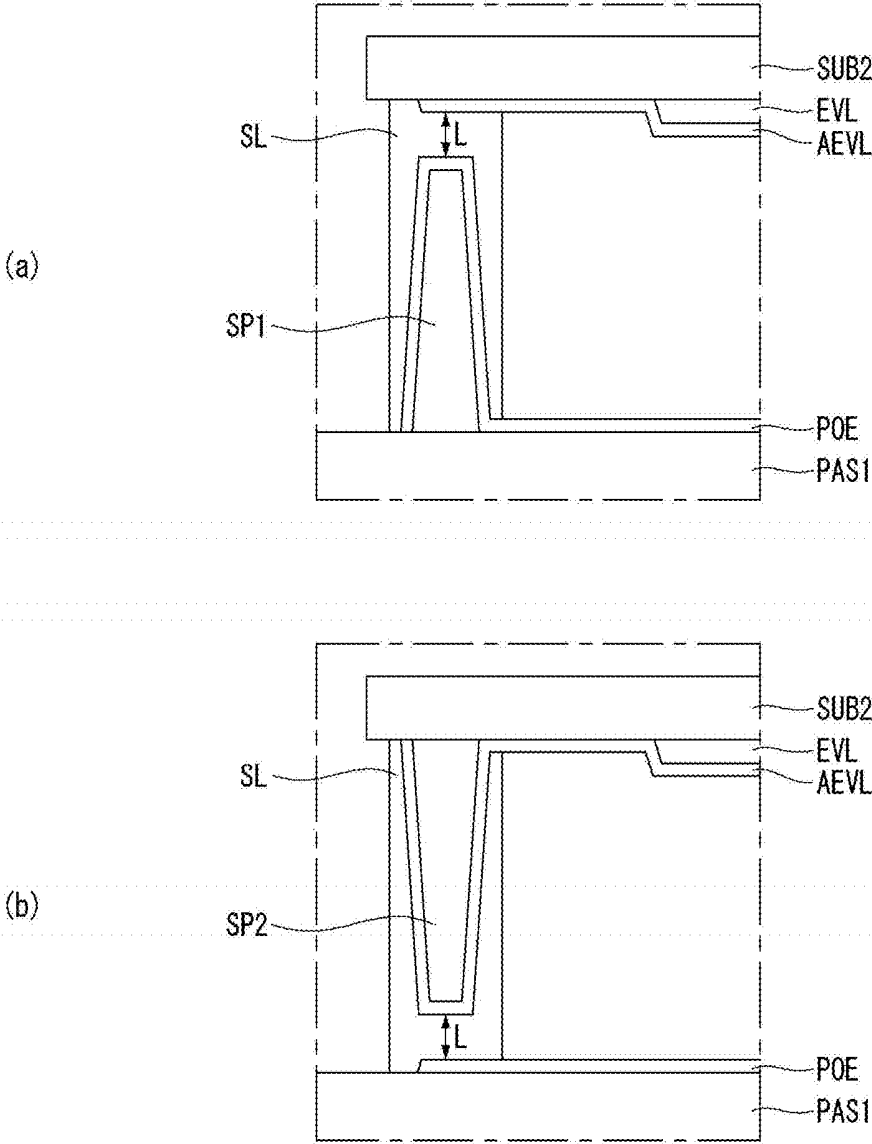


FIG. 10

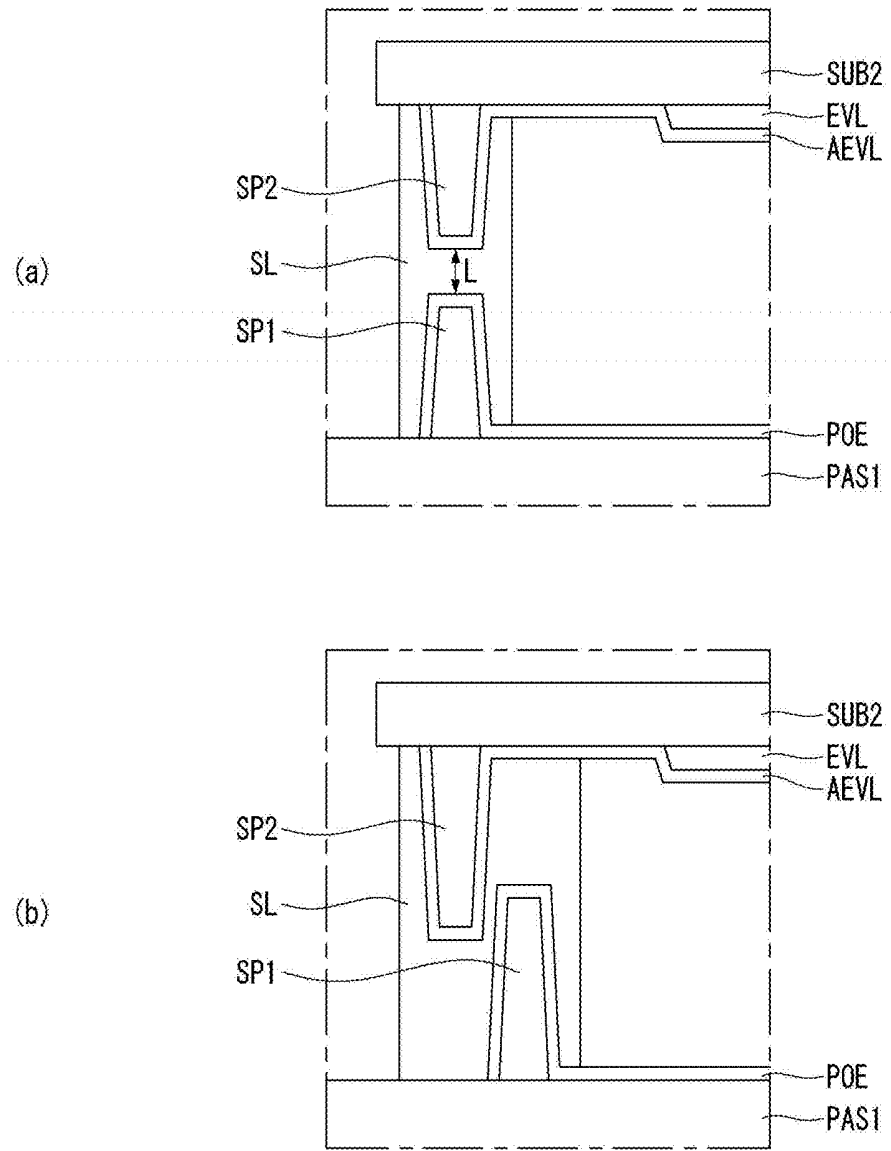
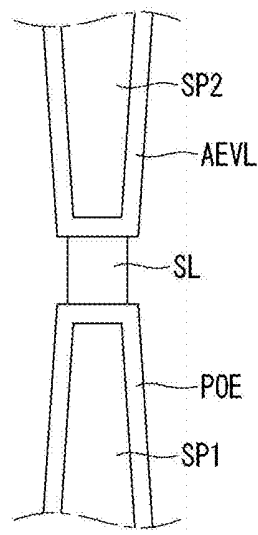


FIG. 11



ORGANIC LIGHT EMITTING DIODE DISPLAY

[0001] This application claims the priority benefit of Korean Patent Application No. 10-2017-0147587 filed on Nov. 7, 2017, which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND

Technical Field

[0002] The present disclosure relates to an organic light emitting diode display.

Discussion of the Related Art

[0003] Various display devices have replaced heavier and larger cathode ray tubes (CRTs). Examples of the display devices may include a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), and an organic light emitting diode (OLED) display.

[0004] In more detail, an OLED display is a self-emission display configured to emit light by exciting an organic compound. The OLED display does not require a backlight unit used in a liquid crystal display and thus has advantages of a thin profile, lightness in weight, and a simpler manufacturing process. The OLED display can be also manufactured at a low temperature and has a fast response time of 1 ms or less, low power consumption, a wide viewing angle, and a high contrast. Thus, the OLED display has been widely used.

[0005] The OLED display includes organic light emitting diodes (OLEDs) converting electric energy into light energy. The OLED includes an anode, a cathode, and an organic emission layer between the anode and the cathode. The OLED display is configured such that the OLED emits light while excitons formed by combining holes from the anode and electrons from the cathode inside an emission layer fall from an excited state to a ground state, and thus displays an image.

[0006] However, a large-area OLED display cannot maintain a uniform luminance throughout an entire surface of an active area, on which an input image is displayed, and generates a luminance variation (or luminance deviation) depending on a position. More specifically, a cathode constituting an organic light emitting diode is formed to cover most of the active area, and there is a problem that a power voltage applied to the cathode does not have a constant voltage value throughout the entire surface of the active area. For example, as a difference between a voltage value at an entrance of the cathode supplied with the power voltage and a voltage value at a position apart from the entrance increases due to a resistance of the cathode, the luminance variation depending on the position increases.

[0007] The problem is more problematic in a top emission type display device. Namely, in the top emission type display device, because it is necessary to secure a transmittance of a cathode positioned at an upper layer of an organic light emitting diode, the cathode is formed of a transparent conductive material such as indium tin oxide (ITO), or an opaque conductive material with a very small thickness. In this instance, because a surface resistance of the cathode increases, a luminance variation depending on a position remarkably increases corresponding to an increase in the surface resistance.

[0008] In order to solve such a problem, a method was proposed to prevent a voltage drop depending on a position by forming a low potential power voltage line including a low resistance material and connecting the low potential power voltage line to a cathode. In the proposed method according to a related art, because the low potential power voltage line was formed on a lower substrate including transistors, one pixel has to further include a connection area of the low potential power voltage line and the cathode in addition to a thin film transistor area and a storage capacitor area. Thus, it was difficult to apply the related art to a high-resolution display including small-sized unit pixels.

SUMMARY

[0009] Accordingly, embodiments of the present disclosure are directed to an organic light emitting diode display that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0010] An aspect of the present disclosure is to provide an organic light emitting diode display capable of achieving a uniform luminance by minimizing a variation in a low potential power voltage depending on a position.

[0011] Additional features and aspects will be set forth in the description that follows, and in part will be apparent from the description, or may be learned by practice of the inventive concepts provided herein. Other features and aspects of the inventive concepts may be realized and attained by the structure particularly pointed out in the written description, or derivable therefrom, and the claims hereof as well as the appended drawings.

[0012] To achieve these and other aspects of the inventive concepts, as embodied and broadly described, an organic light emitting diode display comprises a first substrate on which a power electrode supplied with a power voltage and an organic light emitting diode are disposed, a second substrate on which a power line is disposed, the second substrate facing the first substrate, a conductive filler layer interposed between the first substrate and the second substrate, the conductive filler layer including a conductive medium electrically connecting a cathode of the organic light emitting diode to the power line, and a conductive sealant disposed at an edge of the first substrate and an edge of the second substrate, the conductive filler layer being accommodated inside the conductive sealant, wherein the conductive sealant electrically connects the power electrode to the power line.

[0013] The second substrate may include an auxiliary power line, of which one surface directly contacts the power line and another surface opposite the one surface directly contacts the conductive filler layer. The conductive sealant may be electrically connected to the power line through the auxiliary power line.

[0014] The auxiliary power line may have an area larger than the power line. The auxiliary power line may include a transparent conductive material.

[0015] The first substrate may include a first spacer that overlaps at least a portion of the conductive sealant and may protrude toward the second substrate. The power electrode may cover at least a portion of a surface of the first spacer.

[0016] The second substrate may include a second spacer that overlaps at least a portion of the conductive sealant and may protrude toward the first substrate. The power line may cover at least a portion of a surface of the second spacer.

[0017] The first substrate may include a first spacer that overlaps at least a portion of the conductive sealant and may protrude toward the second substrate. The second substrate may include a second spacer that overlaps at least a portion of the conductive sealant and protrudes toward the first substrate. The power electrode may cover at least a portion of a surface of the first spacer. The power line may cover at least a portion of a surface of the second spacer.

[0018] An upper surface of the first spacer may face an upper surface of the second spacer.

[0019] The first spacer and the second spacer may be disposed to be interlocked with each other, and one side surface of the first spacer faces one side surface of the second spacer.

[0020] The conductive sealant may be locally disposed in an overlap portion of the first spacer and the second spacer between the first spacer and the second spacer.

[0021] The organic light emitting diode may include an anode and an organic light emitting layer interposed between the anode and the cathode. The organic light emitting layer and the cathode on the first substrate may be disposed to expose the power electrode. An exposed portion of the power electrode may directly contact the conductive filler layer.

[0022] One end of the cathode may extend further than one end of the organic light emitting layer and may directly contact the power electrode.

[0023] The first substrate may include an auxiliary electrode, a barrier disposed on the auxiliary electrode, a cathode included in the organic light emitting diode and divided by the barrier, the cathode exposing at least a portion of the auxiliary electrode, one end of the cathode directly contacting the auxiliary electrode, and a protective layer disposed on the cathode and divided by the barrier, the protective layer exposing at least a portion of the auxiliary electrode, one end of the protective layer directly contacting the auxiliary electrode. The conductive filler layer may be connected to the cathode through the auxiliary electrode.

[0024] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the inventive concepts as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, that may be included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate embodiments of the disclosure and together with the description serve to explain various principles of the disclosure.

[0026] FIG. 1 is a block diagram schematically illustrating an organic light emitting diode (OLED) display according to an embodiment of the disclosure.

[0027] FIG. 2 schematically illustrates configuration of a pixel shown in FIG. 1.

[0028] FIG. 3 is a cross-sectional view of an OLED display according to a first embodiment of the disclosure.

[0029] FIG. 4 is a cross-sectional view of an OLED display according to a second embodiment of the disclosure.

[0030] FIG. 5 is an enlarged view of an area AR1 shown in FIG. 4.

[0031] FIG. 6 illustrates cross-sectional views schematically illustrating a shape of a barrier.

[0032] FIG. 7 is a cross-sectional view of an OLED display according to a third embodiment of the disclosure.

[0033] FIGS. 8 to 11 illustrate a power supply path using a sealant in an OLED display according to a fourth embodiment of the disclosure.

DETAILED DESCRIPTION

[0034] Reference will now be made in detail to embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. Detailed descriptions of known arts will be omitted if such may mislead the embodiments of the disclosure. In describing various embodiments, the same components may be described in a first embodiment, and a description thereof may be omitted in other embodiments.

[0035] The terms “first,” “second,” etc. may be used to describe various components, but the components are not limited by such terms. The terms are used only for the purpose of distinguishing one component from other components.

[0036] FIG. 1 is a block diagram schematically illustrating an organic light emitting diode (OLED) display according to an embodiment of the disclosure. FIG. 2 schematically illustrates configuration of a pixel shown in FIG. 1.

[0037] Referring to FIG. 1, an OLED display 10 according to an embodiment of the disclosure includes a display driving circuit and a display panel DIS.

[0038] The display driving circuit includes a data driving circuit 12, a gate driving circuit 14, and a timing controller 16. The display driving circuit applies a video data voltage of an input image to pixels of the display panel DIS. The data driving circuit 12 converts digital video data RGB received from the timing controller 16 into an analog gamma compensation voltage and generates a data voltage. The data voltage output from the data driving circuit 12 is supplied to data lines D1 to Dm, where m is a positive integer. The gate driving circuit 14 sequentially supplies a gate signal synchronized with the data voltage to gate lines G1 to Gn and selects pixels of the display panel DIS to which the data voltage is applied, where n is a positive integer.

[0039] The timing controller 16 receives timing signals, such as a vertical sync signal Vsync, a horizontal sync signal Hsync, a data enable signal DE, and a main clock MCLK, from a host system 19 and synchronizes operation timing of the data driving circuit 12 with operation timing of the gate driving circuit 14. A data timing control signal for controlling the data driving circuit 12 includes a source sampling clock SSC, a source output enable signal SOE, and the like. A gate timing control signal for controlling the gate driving circuit 14 includes a gate start pulse GSP, a gate shift clock GSC, a gate output enable signal GOE, and the like.

[0040] The host system 19 may be one of a television system, a set-top box, a navigation system, a DVD player, a Blu-ray player, a personal computer (PC), a home theater system, a phone system, and other systems that include or operate in conjunction with a display. The host system 19 includes a system-on chip (SoC), in which a scaler is embedded, and converts the digital video data RGB of the input image into a format suitable for displaying the input image on the display panel DIS. The host system 19 trans-

mits the digital video data RGB of the input image and the timing signals Vsync, Hsync, DE and MCLK to the timing controller 16.

[0041] The display panel DIS includes a pixel array. The pixel array includes the pixels defined by the data lines D1 to Dm and the gate lines G1 to Gn. Each pixel includes an organic light emitting diode serving as a self-emission element.

[0042] Referring to FIG. 2, the display panel DIS includes a plurality of data lines D, a plurality of gate lines G intersecting the data lines D, and pixels respectively arranged at intersections of the data lines D and the gate lines G in a matrix. Each pixel includes an organic light emitting diode, a driving thin film transistor (TFT) DT for controlling an amount of current flowing through the organic light emitting diode, and a programming unit SC for setting a gate-to-source voltage of the driving thin film transistor DT.

[0043] The programming unit SC may include at least one switching thin film transistor and at least one storage capacitor. The switching thin film transistor is turned on in response to a gate signal from the gate line G to thereby apply a data voltage from the data line D to one electrode of the storage capacitor. The driving thin film transistor DT controls an amount of current supplied to the organic light emitting diode depending on a magnitude of voltage stored in the storage capacitor, thereby controlling an amount of light emitted by the organic light emitting diode. The amount of light emitted by the organic light emitting diode is proportional to the amount of current supplied from the driving thin film transistor DT. The pixel is connected to a high potential power voltage source and a low potential power voltage source and receives a high potential power voltage EVDD and a low potential power voltage EVSS from a power generator (not shown). The thin film transistors constituting the pixel may be p-type thin film transistors or n-type thin film transistors. Further, semiconductor layers of the thin film transistors constituting the pixel may include amorphous silicon, polycrystalline silicon, or oxide. In the following description, embodiments of the disclosure use a semiconductor layer including oxide as an example. The organic light emitting diode includes an anode ANO, a cathode CAT, and an organic light emitting layer between the anode ANO and the cathode CAT. The anode ANO is connected to the driving thin film transistor DT.

First Embodiment

[0044] FIG. 3 is a cross-sectional view of an OLED display according to a first embodiment of the disclosure.

[0045] Referring to FIG. 3, an OLED display according to a first embodiment of the disclosure includes a display panel including a first substrate SUB1 and a second substrate SUB2 facing each other and a conductive filler layer CFL between the first substrate SUB1 and the second substrate SUB2. The first substrate SUB1 is a thin film transistor array substrate on which a thin film transistor T and an organic light emitting diode OLE are disposed. The second substrate SUB2 is a substrate on which a low potential power voltage line (hereinafter referred to as "Evss line") EVL is disposed. The second substrate SUB2 may function as an encapsulation substrate. The first substrate SUB1 and the second substrate SUB2 may be attached to each other using a sealant SL. The sealant SL is disposed at an edge of the first substrate SUB1 and an edge of the second substrate SUB2

and maintains a predetermined attachment distance between the first substrate SUB1 and the second substrate SUB2. The conductive filler layer CFL may be disposed inside the sealant SL.

[0046] The first substrate SUB1 may be made of glass material or plastic material. For example, the first substrate SUB1 may be made of plastic material such as polyimide (PI), polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polycarbonate (PC) and may have flexible characteristics.

[0047] The thin film transistor T and the organic light emitting diode OLE connected to the thin film transistor T are formed on the first substrate SUB1. A light shielding layer LS and a buffer layer BUF may be formed between the first substrate SUB1 and the thin film transistor T. The light shielding layer LS is disposed to overlap a semiconductor layer, particularly, a channel of the thin film transistor T and can protect an oxide semiconductor element from external light. The buffer layer BUF can block ions or impurities diffused from the first substrate SUB1 and also block moisture penetration from the outside.

[0048] The thin film transistor T includes a semiconductor layer ACT, a gate electrode GE, a source electrode SE, and a drain electrode DE.

[0049] A gate insulating layer GI and the gate electrode GE are disposed on the semiconductor layer ACT. The gate insulating layer GI functions to insulate the gate electrode GE and may be formed of silicon oxide (SiOx). However, embodiments are not limited thereto. The gate electrode GE is disposed to overlap the semiconductor layer ACT with the gate insulating layer GI interposed therebetween. The gate electrode GE may be formed as a single layer or a multilayer using copper (Cu), molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), tantalum (Ta), tungsten (W), or a combination thereof. The gate insulating layer GI and the gate electrode GE may be patterned using the same mask. In this instance, the gate insulating layer GI and the gate electrode GE may have the same area. Although not shown, the gate insulating layer GI may be formed to cover the entire surface of the first substrate SUB1.

[0050] An interlayer dielectric layer IN is positioned on the gate electrode GE. The interlayer dielectric layer IN functions to insulate the gate electrode GE and the source and drain electrodes SE and DE from each other. The interlayer dielectric layer IN may be formed of silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof. However, embodiments are not limited thereto.

[0051] The source electrode SE and the drain electrode DE are positioned on the interlayer dielectric layer IN. The source electrode SE and the drain electrode DE are spaced from each other by a predetermined distance. The source electrode SE contacts one side of the semiconductor layer ACT through a source contact hole penetrating the interlayer dielectric layer IN. The drain electrode DE contacts the other side of the semiconductor layer ACT through a drain contact hole penetrating the interlayer dielectric layer IN.

[0052] Each of the source electrode SE and the drain electrode DE may be formed as a single layer or as a multilayer. When each of the source electrode SE and the drain electrode DE is formed as the single layer, each of the source electrode SE and the drain electrode DE may be formed of molybdenum (Mo), aluminum (Al), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd),

copper (Cu), or a combination thereof. When each of the source electrode SE and the drain electrode DE is formed as the multilayer, each of the source electrode SE and the drain electrode DE may be formed as a double layer of Mo/Al-Nd, Mo/Al, Ti/Al or Cu/MoTi, or as a triple layer of Mo/Al-Nd/Mo, Mo/Al/Mo, Ti/Al/Ti or MoTi/Cu/MoTi.

[0053] A passivation layer PAS1 is positioned on the thin film transistor T. The passivation layer PAS1 protects the thin film transistor T and may be formed of silicon oxide (SiOx), silicon nitride (SiNx), or a multilayer thereof.

[0054] A planarization layer OC is positioned on the passivation layer PAS1. The planarization layer OC can reduce or planarize a height difference (or step coverage) of an underlying structure and may be formed of an organic material such as photo acryl, polyimide, benzocyclobutene-based resin, and acrylate-based resin. If necessary or desired, one of the passivation layer PAS1 and the planarization layer OC may be omitted.

[0055] The organic light emitting diode OLE are positioned on the planarization layer OC. The organic light emitting diode OLE includes an anode ANO, an organic light emitting layer OL, and a cathode CAT.

[0056] More specifically, the anode ANO is positioned on the planarization layer OC. The anode ANO is connected to the source electrode SE of the thin film transistor T through a contact hole penetrating the passivation layer PAS1 and the planarization layer OC. The anode ANO may include a reflective layer and thus serve as a reflective electrode. The reflective layer may be formed of aluminum (Al), copper (Cu), silver (Ag), palladium (Pd), nickel (Ni), or a combination thereof. For example, the reflective layer may be formed of Ag/Pd/Cu (APC) alloy. The anode ANO may be formed as a multilayer including a reflective layer.

[0057] A bank layer BN is positioned on the first substrate SUB1, on which the anode ANO is formed, and partitions pixels. The bank layer BN may be formed of an organic material such as polyimide, benzocyclobutene-based resin, and acrylate. A center portion of the anode ANO exposed by the bank layer BN may be defined as an emission region.

[0058] The bank layer BN may be configured to expose the center portion of the anode ANO and cover an edge of the anode ANO. The exposed portion of the anode ANO may be designed to have as large an area as possible, in order to sufficiently secure an aperture ratio.

[0059] The bank layer BN and the planarization layer OC may be patterned to cover only the thin film transistor T and a storage capacitor Cst connected to the thin film transistor T inside the pixel. As shown in FIG. 3, the storage capacitor Cst may have a triple structure in which first to third capacitor electrodes are stacked. However, embodiments are not limited thereto. For example, the storage capacitor Cst may be implemented as a plurality of layers.

[0060] The organic light emitting layer OL is positioned on the first substrate SUB1 on which the bank layer BN is formed. The organic light emitting layer OL may be widely formed on a front surface of the first substrate SUB1. The organic light emitting layer OL is a layer, in which electrons and holes combine and emit light. The organic light emitting layer OL includes an emission layer EML and may further include one or more of common layers such as a hole injection layer HIL, a hole transport layer HTL, an electron transport layer ETL, and an electron injection layer EIL. The emission layer EML may include a light emitting material that generates white light.

[0061] The organic light emitting layer OL emitting white light may have a multi-stack structure, for example, an n-stack structure, where n is an integer equal to or greater than 1. For example, 2-stack structure may include a charge generation layer CGL between the anode ANO and the cathode CAT and a first stack and a second stack respectively disposed on and under the charge generation layer CGL. Each of the first stack and the second stack includes an emission layer and may further include at least one common layer. The emission layer of the first stack and the emission layer of the second stack may include emission materials of different colors, respectively.

[0062] The cathode CAT is positioned on the organic light emitting layer OL. The cathode CAT may be widely formed on the front surface of the first substrate SUB1. The cathode CAT may be formed of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO). Alternatively, the cathode CAT may be formed of a material, which is thin enough to transmit light, for example, magnesium (Mg), calcium (Ca), aluminum (Al), silver (Ag), or a combination thereof.

[0063] The Evss line EVL and a color filter CF are formed on the second substrate SUB2. A stacking order of the Evss line EVL and the color filter CF on the second substrate SUB2 may be changed. For example, the color filter CF may be formed after the Evss line EVL is formed, or the Evss line EVL may be formed after the color filter CF is formed.

[0064] The Evss line EVL includes a low resistance conductive material. For example, the Evss line EVL may be formed of molybdenum (Mo), aluminum (Al), chromium (Cr), gold (Au), titanium (Ti), nickel (Ni), neodymium (Nd), copper (Cu), or a combination thereof.

[0065] The Evss line EVL may include a low reflective conductive material. For example, the Evss line EVL is formed of the low reflective conductive material and thus can prevent visibility from being reduced by the reflection of external light. Thus, a display device according to embodiments of the disclosure does not need to include a separate component for shielding (or absorbing) light incident from outside, like a polarizing film.

[0066] The Evss line EVL may function as a black matrix. Therefore, the Evss line EVL can prevent a defect of color mixture from occurring between neighboring pixels. The Evss line EVL may be disposed corresponding to a non-emission region so as to expose at least the emission region. Further, the first embodiment of the disclosure can use the Evss line EVL as the black matrix and thus does not need to additionally perform a separate process for forming the black matrix. Therefore, the first embodiment of the disclosure can further reduce the number of processes compared to a related art structure, and thus can reduce the manufacturing time and the manufacturing cost and remarkably improve product yield.

[0067] The color filter CF may include red (R), blue (B), and green (G) color filters. The pixel may include subpixels emitting red, blue, and green light, and the color filters CF may be respectively assigned to the corresponding subpixels. The red, blue, and green color filters CF may be partitioned by the Evss line EVL. If necessary or desired, the pixel may further include a white (W) subpixel.

[0068] The conductive filler layer CFL is interposed between the first substrate SUB1 and the second substrate SUB2 and includes a conductive medium. The conductive filler layer CFL may be formed by dispersing conductive

fillers in a solvent. Alternatively, the conductive filler layer CFL may include a conductive solvent. For example, the conductive filler layer CFL may include at least one of poly(3,4-ethylenedioxythiophene) (PEDOT) which is a conductive polymer, and an ionic liquid. However, embodiments are not limited thereto.

[0069] The attachment distance between the first substrate SUB1 and the second substrate SUB2 may be appropriately selected depending on viscosity of the conductive filler layer CFL. Because the embodiment of the disclosure uses the conductive fillers having lower viscosity than non-conductive fillers, the distance between the first substrate SUB1 and the second substrate SUB2 can be reduced. Hence, the embodiment of the disclosure can secure a wide viewing angle and a high aperture ratio. The cathode CAT of the first substrate SUB1 and the Evss line EVL of the second substrate SUB2 are electrically connected through the conductive filler layer CFL. Thus, the low potential power voltage is applied to both the cathode CAT and the Evss line EVL.

[0070] The first embodiment of the disclosure can reduce a voltage variation (or voltage deviation) depending on a position by connecting the Evss line EVL formed of the low resistance conductive material to the cathode CAT. Hence, the first embodiment of the disclosure can reduce non-uniformity of luminance or a luminance variation (or luminance variation).

[0071] The first embodiment of the disclosure does not need to separately assign an area for forming the Evss line EVL and an area for connecting the Evss line EVL and the cathode CAT to the thin film transistor array substrate, as in the related art. Therefore, the first embodiment of the disclosure can be easily applied to a high-resolution display having a high pixel per inch (PPI) and can remarkably improve a degree of design freedom.

[0072] A supply path of the low potential power voltage generated by a power generator (not shown) is described in detail below.

[0073] The OLED display according to the first embodiment of the disclosure further includes a connection member LM attached to at least one side of the first substrate SUB1. The connection member LM may be a chip-on film (COF). However, embodiments are not limited thereto.

[0074] The first substrate SUB1 includes a low potential power voltage pad (hereinafter referred to as "Evss pad") EVP and a power electrode POE. The Evss pad EVP is disposed outside the sealant SL and is electrically connected to the connection member LM. The power electrode POE is disposed inside the sealant SL and is electrically connected to the conductive filler layer CFL.

[0075] The Evss pad EVP receives the low potential power voltage generated by the power generator (not shown) through the connection member LM and transfers the received low potential power voltage to the power electrode POE. The power electrode POE then transfers the low potential power voltage to the conductive filler layer CFL.

[0076] Namely, the connection member LM, the Evss pad EVP, the power electrode POE, the conductive filler layer CFL, and the cathode CAT may be electrically connected to form a low potential power voltage supply path, and/or the connection member LM, the Evss pad EVP, the power electrode POE, the conductive filler layer CFL, the Evss line EVL, and the cathode CAT may be electrically connected to form a low potential power voltage supply path.

[0077] More specifically, the Evss pad EVP includes at least one pad electrode. In the case where a plurality of pad electrodes are used, the pad electrodes may be disposed at different layers with at least one insulating layer interposed therebetween and may be electrically connected through a pad contact hole penetrating the at least one insulating layer. For example, as shown in FIG. 3, the Evss pad EVP may include a first pad electrode PE1 and a second pad electrode PE2 that are disposed at different layers with the passivation layer PAS1 interposed therebetween, and the first pad electrode PE1 and the second pad electrode PE2 may be connected to each other through a first pad contact hole PH1 penetrating the passivation layer PAS1. Hereinafter, the embodiment of the disclosure describes a case where the Evss pad EVP includes the first pad electrode PE1 and the second pad electrode PE2 as an example, for convenience of explanation.

[0078] The first pad electrode PE1 is disposed outside the sealant SL and is exposed to the outside. The exposed first pad electrode PE1 may be attached to the connection member LM. The first pad electrode PE1 and the connection member LM may be attached to each other through an anisotropic conductive film (ACF) layer (not shown) interposed between them.

[0079] The second pad electrode PE2 is extended to the inside of the sealant SL and is electrically connected to the power electrode POE. In this instance, the second pad electrode PE2 may contact the power electrode POE through a second pad contact hole PH2 penetrating the passivation layer PAS1. FIG. 3 illustrates that the second pad electrode PE2 and the power electrode POE are disposed with only the passivation layer PAS1 interposed therebetween, by way of example. However, embodiments are not limited thereto. For example, the second pad electrode PE2 and the power electrode POE may be disposed at different layers with the passivation layer PAS1 and the planarization layer OC interposed therebetween and may be electrically connected to each other through a contact hole penetrating the passivation layer PAS1 and the planarization layer OC.

[0080] The power electrode POE may be formed together when the anode ANO is formed. Namely, the power electrode POE may be formed of the same material as the anode ANO. However, embodiments are not limited thereto.

[0081] At least a portion of the power electrode POE may be exposed and may directly contact the conductive filler layer CFL. In order to expose at least a portion of the power electrode POE, respective areas of layers widely formed on the front surface of the first substrate SUB1 may be controlled. The layers, of which the area is controllable, may be layers (e.g., the organic light emitting layer OL and the cathode CAT) formed after the formation of the power electrode POE.

[0082] More specifically, the above layers are formed using a frame-shaped open mask (not shown) having an opening. An area of the opening of the open mask may correspond to an area occupied by the above layers on the first substrate SUB1. Thus, at least a portion of the power electrode POE can be exposed by controlling the area of the opening of the open mask. The exposed portion of the power electrode POE may directly contact the conductive filler layer CFL and supply the low potential power voltage to the conductive filler layer CFL. Hence, a power supply path connecting the connection member LM, the Evss pad EVP, and the conductive filler layer CFL may be formed. Through

the power supply path, the low potential power voltage can be supplied to the Evss line EVL of the second substrate SUB2 and supplied to the cathode CAT of the first substrate SUB1.

[0083] The cathode CAT on the power electrode POE may cover the organic light emitting layer OL, and one end of the cathode CAT may extend more than one end of the organic light emitting layer OL and directly contact the power electrode POE. Namely, one end of the cathode CAT may directly contact an exposed upper surface of the power electrode POE. Hence, a power supply path connecting the connection member LM, the Evss pad EVP, and the cathode CAT may be formed.

[0084] The first embodiment of the disclosure may form a plurality of power supply paths for supplying the low potential power voltage to the Evss line EVL of the second substrate SUB2. Namely, the first embodiment of the disclosure can electrically connect the power electrode POE of the first substrate SUB1 to the Evss line EVL of the second substrate SUB2 using the sealant SL, in order to secure an addition power supply path in addition to a power supply path formed by connecting the power electrode POE of the first substrate SUB1 and the Evss line EVL of the second substrate SUB2 through the conductive filler layer CFL.

[0085] More specifically, the sealant SL according to the first embodiment of the disclosure may be a conductive sealant. The conductive sealant SL may be configured to mix a conductive material in a solvent. For example, the solvent may include an epoxy-based resin, a phenol-based resin, an acryl-based resin, a combination of a thermosetting and photocurable resin and an organic binder, and the like. The conductive material may include graphite, a metal powder, and the like. One end of the conductive sealant SL is connected to the power electrode POE of the first substrate SUB1, and another end of the conductive sealant SL is connected to the Evss line EVL of the second substrate SUB2. The conductive sealant SL may be formed to cover one end of the power electrode POE and one end of the Evss line EVL, so that the power electrode POE and the Evss line EVL are not exposed to the outside.

[0086] Hence, in addition to a power supply path connecting the connection member LM, the Evss pad EVP, the conductive filler layer CFL, and the Evss line EVL, a power supply path connecting the connection member LM, the Evss pad EVP, the sealant SL, and the Evss line EVL may be formed. The first embodiment of the disclosure can easily supply the low potential power voltage to the Evss line EVL of the second substrate SUB2 by sufficiently securing the power supply path.

Second Embodiment

[0087] FIG. 4 is a cross-sectional view of an OLED display according to a second embodiment of the disclosure. FIG. 5 is an enlarged view of an area AR1 shown in FIG. 4. Description of structures and components identical or equivalent to those illustrated in the first embodiment is omitted in the second embodiment.

[0088] Referring to FIGS. 4 and 5, the OLED display according to the second embodiment of the disclosure further includes a protective layer PAS2 for preventing the deterioration of an organic light emitting diode OLE. The protective layer PAS2 is positioned on a cathode CAT. The protective layer PAS2 may be widely formed on a front

surface of a first substrate SUB1. The protective layer PAS2 may be formed of a material such as silicon oxide (SiOx) and silicon nitride (SiNx).

[0089] The protective layer PAS2 is positioned on the cathode CAT and can block the penetration of foreign material that may enter the organic light emitting diode OLE. For example, because the cathode CAT including a transparent conductive material is a crystalline component and cannot block the penetration of ions and moisture, ionic components or external impurities of an ionic liquid included in a conductive filler layer CFL may pass through the cathode CAT and may enter the organic light emitting layer OL. The second embodiment of the disclosure further includes the protective layer PAS2 on the organic light emitting diode OLE and can block the penetration of foreign material that may enter the organic light emitting diode OLE. Hence, the second embodiment of the disclosure can prevent a reduction in lifespan of the organic light emitting diode OLE and a luminance reduction.

[0090] In addition, the protective layer PAS2 is positioned on the cathode CAT and can buffer or mitigate a stress applied to the cathode CAT when the first substrate SUB1 and a second substrate SUB2 are attached to each other. For example, because the cathode CAT including the transparent conductive material has brittle characteristics, the cathode CAT may easily crack due to an external force applied. The second embodiment of the disclosure further includes the protective layer PAS2 on the cathode CAT and can prevent a crack from being generated in the cathode CAT. Furthermore, the second embodiment of the disclosure can prevent the penetration of oxygen or moisture through the crack.

[0091] The conductive filler layer CFL may include an ionic liquid. In this instance, the ionic liquid may directly contact the cathode CAT, causing a defect that the cathode CAT is oxidized. The second embodiment of the disclosure can prevent the deterioration of the cathode CAT by interposing the protective layer PAS2 between the cathode CAT and the conductive filler layer CFL.

[0092] In the second embodiment of the disclosure, because the protective layer PAS2 is interposed between the conductive filler layer CFL and the cathode CAT, the conductive filler layer CFL and the cathode CAT cannot be connected to each other. The second embodiment of the disclosure includes an auxiliary electrode AE and a barrier BR on the auxiliary electrode AE, in order to electrically connect the conductive filler layer CFL to the cathode CAT.

[0093] The auxiliary electrode AE is positioned on a planarization layer OC. The auxiliary electrode AE may be formed of the same material as the anode ANO at the same layer as the anode ANO. In this instance, because a separate process for forming the auxiliary electrode AE does not need to be performed, the number of processes can be reduced. Hence, the manufacturing time and the manufacturing cost can be reduced, and product yield can be remarkably improved.

[0094] A bank layer BN on the auxiliary electrode AE may be configured to expose a center portion of the auxiliary electrode AE and cover an edge of the auxiliary electrode AE. The exposed portion of the auxiliary electrode AE may be designed to have as large an area as possible, in order to sufficiently secure a contact area between the auxiliary electrode AE and the conductive filler layer CFL.

[0095] The barrier BR is positioned on the auxiliary electrode AE. The barrier BR functions to physically divide

each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 that will be formed later. In other words, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 is disposed on the auxiliary electrode AE and is physically divided by the barrier BR. Hence, each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2 may be discontinuously formed on the auxiliary electrode AE.

[0096] More specifically, the organic light emitting layer OL on the auxiliary electrode AE is physically divided by the barrier BR. The organic light emitting layer OL is divided by the barrier BR and exposes at least a portion of the auxiliary electrode AE around the barrier BR. A portion of the organic light emitting layer OL divided by the barrier BR is positioned on the barrier BR.

[0097] The cathode CAT on the auxiliary electrode AE is physically divided by the barrier BR. The cathode CAT is divided by the barrier BR and exposes at least a portion of the auxiliary electrode AE around the barrier BR. A portion of the cathode CAT divided by the barrier BR is positioned on the barrier BR.

[0098] The cathode CAT covers the organic light emitting layer OL, and one end of the cathode CAT directly contacts the auxiliary electrode AE. Namely, one end of the cathode CAT, which is divided by the barrier BR and is exposed, directly contacts an exposed upper surface of the auxiliary electrode AE. Such a structure may be implemented by a step coverage difference between materials forming the organic light emitting layer OL and the cathode CAT. For example, because the cathode CAT is made of a transparent conductive material having better step coverage than a formation material of the organic light emitting layer OL, the cathode CAT may be configured to directly contact the auxiliary electrode AE. Furthermore, in order to implement the structure, the organic light emitting layer OL and the cathode CAT may be formed using different methods. For example, the organic light emitting layer OL may be formed using a thermal deposition method, and the cathode CAT may be formed using a sputtering method. Hence, one end of the divided cathode CAT may be extended further than one end of the divided organic light emitting layer OL and may directly contact the auxiliary electrode AE.

[0099] The protective layer PAS2 on the auxiliary electrode AE is physically divided by the barrier BR. The protective layer PAS2 is divided by the barrier BR and exposes at least a portion of the auxiliary electrode AE around the barrier BR. A portion of the protective layer PAS2 divided by the barrier BR is positioned on the barrier BR. Hence, the portion of the organic light emitting layer OL, the portion of the cathode CAT, and the portion of the protective layer PAS2, each of which is divided by the barrier BR, are sequentially stacked on the barrier BR.

[0100] The second embodiment of the disclosure includes the barrier BR and thus can expose at least a portion of the auxiliary electrode AE while physically dividing each of the organic light emitting layer OL, the cathode CAT, and the protective layer PAS2. The exposed portion of the auxiliary electrode AE can directly contact the conductive filler layer CFL to receive the low potential power voltage from the Evss line EVL of the second substrate SUB2, and can also directly contact the cathode CAT to transfer the received low potential power voltage to the cathode CAT.

[0101] With reference to FIG. 6, an example of a shape of a barrier according to an embodiment of the disclosure is described below. FIG. 6 illustrates cross-sectional views schematically illustrating a shape of a barrier.

[0102] A barrier BR may be formed as a double layer including a first structure B1 and a second structural B2. The first structure B1 may be disposed on the second structural B2, and an edge of the first structure B1 may have an eaves shape. Namely, the edge of the first structure B1 may protrude from an edge of the second structural B2 to the outside by a predetermined distance RR. The distance RR between the edge of the first structure B1 and the edge of the second structural B2 may be properly selected so that the barrier BR can expose at least a portion of an auxiliary electrode AE while dividing each of an organic light emitting layer, a cathode, and a protective layer. In other words, each of the organic light emitting layer OL (see FIG. 4), the cathode CAT (see FIG. 4), and the protective layer PAS2 (see FIG. 4) is patterned to expose at least a portion of the auxiliary electrode AE while being divided around the barrier BR due to the predetermined distance RR between the edge of the first structure B1 and the edge of the second structural B2. The first structure B1 may have a reverse taper shape as shown in part (a) of FIG. 6 and may have a taper shape as shown in part (b) of FIG. 6. The first structure B1 and the second structural B2 may be formed of different materials.

[0103] A barrier BR may be formed as a single layer including a first structure B1. In this instance, the first structure B1 has a shape in which an edge of an upper side protrudes from an edge of a lower side to the outside by a predetermined distance RR. For example, the first structure B1 may have a reverse taper shape as shown in part (c) of FIG. 6. Namely, a vertical cross-sectional shape of the first structure B1 may have a trapezoidal shape, the upper side may have a length longer than the lower side, and one end of the upper side may protrude from one end of the lower side to the outside by the predetermined distance RR. The distance RR between one end of the upper side and one end of the lower side may be properly selected so that the barrier BR can expose at least a portion of an auxiliary electrode AE while dividing each of an organic light emitting layer, a cathode, and a protective layer. In other words, each of the organic light emitting layer OL (see FIG. 4), the cathode CAT (see FIG. 4), and the protective layer PAS2 (see FIG. 4) is patterned to expose at least a portion of the auxiliary electrode AE while being divided around the barrier BR due to the distance RR between one end of the upper side and one end of the lower side.

Third Embodiment

[0104] FIG. 7 is a cross-sectional view of an OLED display according to a third embodiment of the disclosure. Description of structures and components identical or equivalent to those illustrated in the first and second embodiments is omitted in the third embodiment.

[0105] Referring to FIG. 7, the OLED display according to the third embodiment of the disclosure includes a first substrate SUB1 (see FIGS. 3 and 4) and a second substrate SUB2 facing each other. An Evss line EVL and an auxiliary Evss line (or referred to as "auxiliary power line") AEVL are formed on the second substrate SUB2. A color filter CF may be positioned on the second substrate SUB2 as in the first

and second embodiments and may be positioned on the first substrate SUB1 if necessary or desired.

[0106] One surface of the auxiliary Evss line AEVL directly contacts the Evss line EVL, and the other surface of the auxiliary Evss line AEVL directly contacts a conductive filler layer CFL. The auxiliary Evss line AEVL is a power line for increasing a contact area between the Evss line EVL and the conductive filler layer CFL and may have an area larger than the Evss line EVL. The auxiliary Evss line AEVL may be interposed between the Evss line EVL and the conductive filler layer CFL. The auxiliary Evss line AEVL may be formed to cover the Evss line EVL and the color filter CF and may be widely formed on a front surface of the second substrate SUB2 including an emission region. The auxiliary Evss line AEVL may be formed of a transparent conductive material such as indium tin oxide (ITO) and indium zinc oxide (IZO).

[0107] Because the third embodiment of the disclosure can sufficiently secure the contact area between the Evss line EVL and the conductive filler layer CFL using the auxiliary Evss line AEVL, the third embodiment of the disclosure can minimize a contact failure between the Evss line EVL and the conductive filler layer CFL. Further, the third embodiment of the disclosure can more efficiently reduce a voltage variation depending on a position and thus can reduce non-uniformity of luminance or a luminance variation.

Fourth Embodiment

[0108] FIGS. 8 to 11 illustrate a power supply path using a sealant in an OLED display according to a fourth embodiment of the disclosure.

[0109] As described above, an embodiment of the disclosure can form an Evss power supply path using a conductive sealant SL. Namely, an embodiment of the disclosure can form a power supply path electrically connecting a power electrode POE on a first substrate SUB1 to an Evss line EVL on a second substrate SUB2 using the conductive sealant SL.

[0110] More specifically, referring to FIG. 8, the conductive sealant SL is interposed between the first substrate SUB1 and the second substrate SUB2 and has a previously set height in order to maintain an attachment distance between the first substrate SUB1 and the second substrate SUB2. One end of the conductive sealant SL is connected to the power electrode POE on the first substrate SUB1, and the other end of the conductive sealant SL is connected to the Evss line EVL on the second substrate SUB2. Hence, the power electrode POE and the Evss line EVL can be electrically connected through the conductive sealant SL. The conductive sealant SL and the Evss line EVL may directly contact and may be electrically connected to each other. Alternatively, the conductive sealant SL and the Evss line EVL may be electrically connected to each other by a medium of an auxiliary Evss line AEVL. Hereinafter, the latter is used as an example.

[0111] When the power electrode POE and the auxiliary Evss line AEVL are spaced from each other and are electrically connected through the conductive sealant SL interposed between them, the supply of a power voltage may not be easily performed by a resistance of the conductive sealant SL. Namely, because the resistance of the conductive sealant SL increases as a distance between the power electrode POE and the auxiliary Evss line AEVL increases, it may be difficult to perform the supply of the power voltage. A method may be considered to reduce the distance between

the first substrate SUB1 and the second substrate SUB2 in consideration of the resistance. However, because the attachment distance between the first substrate SUB1 and the second substrate SUB2 needs to be fixed to a previously set distance in consideration of characteristics of display devices, there is a limit to adjusting the attachment distance.

[0112] Referring to FIG. 9, the OLED display includes a spacer overlapping at least a portion of the conductive sealant SL in order to reduce the distance between the power electrode POE and the auxiliary Evss line AEVL.

[0113] As shown in part (a) of FIG. 9, a first spacer SP1 may be formed on the first substrate SUB1 and may have a shape protruding toward the second substrate SUB2. An upper surface of the first spacer SP1 may be positioned adjacent to the auxiliary Evss line AEVL. The first spacer SP1 is disposed below the power electrode POE and overlaps the conductive sealant SL.

[0114] The power electrode POE is extended to cover the first spacer SP1. Part (a) of FIG. 9 illustrates that the power electrode POE completely covers the first spacer SP1, by way of example. However, embodiments are not limited thereto. For example, the power electrode POE may be extended to cover at least a portion of the first spacer SP1 so that the power electrode POE is positioned adjacent to the auxiliary Evss line AEVL of the second substrate SUB2. Further, the power electrode POE may be extended up to a most protruding portion (e.g., an upper surface) of the first spacer SP1.

[0115] As shown in part (b) of FIG. 9, a second spacer SP2 may be formed on the second substrate SUB2 and may have a shape protruding toward the first substrate SUB1. An upper surface of the second spacer SP2 may be positioned adjacent to the power electrode POE. The second spacer SP2 is disposed to overlap the conductive sealant SL below the auxiliary Evss line AEVL.

[0116] The auxiliary Evss line AEVL is extended to cover the second spacer SP2. Part (b) of FIG. 9 illustrates that the auxiliary Evss line AEVL completely covers the second spacer SP2, by way of example. However, embodiments are not limited thereto. For example, the auxiliary Evss line AEVL may be extended to cover at least a portion of the second spacer SP2 so that the auxiliary Evss line AEVL is positioned adjacent to the power electrode POE of the first substrate SUB1. Further, the auxiliary Evss line AEVL may be extended up to a most protruding portion (e.g., an upper surface) of the second spacer SP2.

[0117] The fourth embodiment of the disclosure includes the spacer and thus can set a distance between the power electrode POE and the auxiliary Evss line AEVL to a minimum value possible in the process. Hence, the fourth embodiment of the disclosure can reduce an influence of the above-described resistance and stably supply the power voltage to the auxiliary Evss line AEVL.

[0118] However, it may be difficult to sufficiently increase a height of the spacer due to limitations of the process. In order to solve this, referring to FIG. 10, the fourth embodiment of the disclosure may include a first spacer SP1 on the first substrate SUB1 and a second spacer SP2 on the second substrate SUB2.

[0119] The first spacer SP1 may be formed on the first substrate SUB1 and may have a shape protruding toward the second substrate SUB2. An upper surface of the first spacer SP1 may be positioned adjacent to the auxiliary Evss line AEVL. The first spacer SP1 is disposed below the power

electrode POE and overlaps the conductive sealant SL. The power electrode POE is extended to cover at least a portion of the first spacer SP1.

[0120] The second spacer SP2 may be formed on the second substrate SUB2 and may have a shape protruding toward the first substrate SUB1. An upper surface of the second spacer SP2 may be positioned adjacent to the power electrode POE. The second spacer SP2 is disposed to overlap the conductive sealant SL below the auxiliary Evss line AEVL. The auxiliary Evss line AEVL is extended to cover at least a portion of the second spacer SP2.

[0121] As shown in part (a) of FIG. 10, the upper surface of the first spacer SP1 may be disposed opposite the upper surface of the second spacer SP2. Alternatively, as shown in part (b) of FIG. 10, the first spacer SP1 and the second spacer SP2 may be disposed to be interlocked with each other, and thus one side surface of the first spacer SP1 may be disposed opposite one side surface of the second spacer SP2.

[0122] Referring to FIG. 11, the fourth embodiment of the disclosure may include a first spacer SP1 on the first substrate SUB1 and a second spacer SP2 on the second substrate SUB2. FIG. 11 illustrates a modified example of part (a) of FIG. 9.

[0123] The conductive sealant SL may be locally disposed in an overlap portion of the first spacer SP1 and the second spacer SP2 between the first spacer SP1 and the second spacer SP2. Thus, an area of the conductive sealant SL may be set to be the same as or less than a facing area of the first spacer SP1 and the second spacer SP2. In this instance, the attachment distance between the first substrate SUB1 and the second substrate SUB2 may be set to a height of the first spacer SP1, a thickness of the power electrode POE, a height of the conductive sealant SL, a thickness of the auxiliary Evss line AEVL, and a height of the second spacer SP2.

[0124] It will be apparent to those skilled in the art that various modifications and variations can be made in the organic light emitting diode display of the present disclosure without departing from the technical idea or scope of the disclosure. Thus, it is intended that the present disclosure cover the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. An organic light emitting diode display, comprising:
 - a first substrate on which a power electrode supplied with a power voltage and an organic light emitting diode are disposed;
 - a second substrate on which a power line is disposed, the second substrate facing the first substrate;
 - a conductive filler layer interposed between the first substrate and the second substrate, the conductive filler layer including a conductive medium electrically connecting a cathode of the organic light emitting diode to the power line; and
 - a conductive sealant disposed at an edge of the first substrate and an edge of the second substrate, the conductive filler layer being accommodated inside the conductive sealant, wherein the conductive sealant electrically connects the power electrode to the power line.
2. The organic light emitting diode display of claim 1, wherein the second substrate includes an auxiliary power line, of which one surface directly contacts the power line and another surface opposite the one surface directly con-

tacts the conductive filler layer, wherein the conductive sealant is electrically connected to the power line through the auxiliary power line.

3. The organic light emitting diode display of claim 2, wherein the auxiliary power line has an area larger than the power line, and

wherein the auxiliary power line includes a transparent conductive material.

4. The organic light emitting diode display of claim 1, wherein the first substrate includes a first spacer that overlaps at least a portion of the conductive sealant and protrudes toward the second substrate,

wherein the power electrode covers at least a portion of a surface of the first spacer.

5. The organic light emitting diode display of claim 1, wherein the second substrate includes a second spacer that overlaps at least a portion of the conductive sealant and protrudes toward the first substrate,

wherein the power line covers at least a portion of a surface of the second spacer.

6. The organic light emitting diode display of claim 1, wherein the first substrate includes a first spacer that overlaps at least a portion of the conductive sealant and protrudes toward the second substrate,

wherein the second substrate includes a second spacer that overlaps at least a portion of the conductive sealant and protrudes toward the first substrate,

wherein the power electrode covers at least a portion of a surface of the first spacer,

wherein the power line covers at least a portion of a surface of the second spacer.

7. The organic light emitting diode display of claim 6, wherein an upper surface of the first spacer faces an upper surface of the second spacer.

8. The organic light emitting diode display of claim 6, wherein the first spacer and the second spacer are disposed to be interlocked with each other, and one side surface of the first spacer faces one side surface of the second spacer.

9. The organic light emitting diode display of claim 6, wherein the conductive sealant is locally disposed in an overlap portion of the first spacer and the second spacer between the first spacer and the second spacer.

10. The organic light emitting diode display of claim 1, wherein the organic light emitting diode includes an anode and an organic light emitting layer interposed between the anode and the cathode,

wherein the organic light emitting layer and the cathode on the first substrate are disposed to expose the power electrode,

wherein an exposed portion of the power electrode directly contacts the conductive filler layer.

11. The organic light emitting diode display of claim 10, wherein one end of the cathode extends further than one end of the organic light emitting layer and directly contacts the power electrode.

12. The organic light emitting diode display of claim 1, wherein the first substrate includes:

an auxiliary electrode;

a barrier disposed on the auxiliary electrode;

a cathode included in the organic light emitting diode and divided by the barrier, the cathode exposing at least a portion of the auxiliary electrode, one end of the cathode directly contacting the auxiliary electrode; and

a protective layer disposed on the cathode and divided by the barrier, the protective layer exposing at least a portion of the auxiliary electrode, one end of the protective layer directly contacting the auxiliary electrode,

wherein the conductive filler layer is connected to the cathode through the auxiliary electrode.

13. An organic light emitting diode display comprising:
a first substrate on which a power electrode supplied with a power voltage and an organic light emitting diode are disposed;

a second substrate on which a power line is disposed, the second substrate facing the first substrate;

a conductive filler layer interposed between the first substrate and the second substrate, the conductive filler layer including a conductive medium; and

a conductive sealant disposed at an edge of the first substrate and an edge of the second substrate, the conductive filler layer being accommodated inside the conductive sealant,

wherein the conductive sealant electrically connects the power electrode to the power line.

14. The organic light emitting diode display of claim **13**, wherein the conductive filler layer electrically connects a cathode of the organic light emitting diode to the power line.

15. The organic light emitting diode display of claim **13**, wherein the conductive filler layer electrically connects the power electrode to the power line.

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专利名称(译)	有机发光二极管显示器		
公开(公告)号	US20190140038A1	公开(公告)日	2019-05-09
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE JOONSUK KIM SEJUNE		
发明人	LEE, JOONSUK KIM, SEJUNE		
IPC分类号	H01L27/32 H01L51/00 H01L51/52		
CPC分类号	H01L2251/5338 H01L27/1225 H01L27/124 H01L27/1255 H01L29/78633 H01L29/7869 H01L27/3276 H01L51/0097 H01L51/5228 H01L51/5246 H01L27/3262 H01L27/3272 H01L27/1248 H01L27/322 H01L27/3253 H01L2251/5315		
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摘要(译)

公开了一种有机发光二极管显示器。有机发光二极管显示器包括：第一基板，其上提供有电源电压的功率电极和有机发光二极管；第二基板，其上设置有电源线，第二基板面对第一基板，导电填充层介于第一基板和第二基板之间，导电填充层包括将有机发光二极管的阴极电连接到电源线的导电介质，以及设置在第一基板的边缘和边缘的导电密封剂在第二基板中，导电填充层容纳在导电密封剂内。导电密封剂将电源电极电连接到电源线。

